WAFER-LEVEL DAMAGE ASSESSMENT BY TEST STRUCTURES

Final Report

JPL Task 660

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A. OBJECTIVE

The objective of this study was to demonstrate on-lab, cost-effective, and nondestructive capabilities of the multipurpose, microelectronic advanced laser scanner for the diagnosis of functional and physical defects on radiation-resistant designs or radiation-hardened microelectronic devices in wafer-level fabrication processes.

B. PROGRESS AND RESULTS

Introduction

Laser scanning systems have been extended to continuous-wavelength lasers ever since a wide range of lasers has become available. However, utilization of the laser scanner in semiconductor devices has been limited to only a few areas, such as solar cell modules [1] and surface analysis of solid-state semiconductor device materials [2]. The technology for scanning, sensing, image processing, and laser manufacturing has become much more mature, opening up several new avenues of application. Scanning technology can now precisely locate a focused probing laser beam onto the exact position most vulnerable to damage at a fast (<1-ms) rate [3] and automatically collect performance parameters from many points on the device, thanks to easy access to personal computers. Various-wavelength laser beams can be focused down to a 1.5-μm spot size, limited only by diffraction effects, making it possible to probe a specific layer of individual transistors by scanning less than 0.1 μm of step-size. These technology advances have made the laser scanner very attractive for utilization in nondestructive lateral and vertical characterization for submicron microelectronic components.

Microelectronic sensor devices employed in spacecraft applications are continuously exposed to the risk of energetic particles. If a cosmic ray or an energetic particle (such as proton) strike occurs, anomalies can range from a change in the analog state of the sensor to damage in the solid-state semiconductor material. These cause changes in efficiency of the device and possible permanent degradation to the device. In some cases, the device parameters (current and voltage) change only for a certain period after the radiation. To counter these problems, some manufacturers have evolved techniques to increase radiation resistance by hardening and by changing the integrated circuit and operational software designs. Testing of radiation sensitivity has, however, proven to be expensive and time consuming.

Charged-particle interactions can also present severe problems to a solid-state electronic system of charge-coupled devices (CCDs) in space, due to the generation of soft and hard errors [4,5]. Proton environments of space are a serious concern of space-imaging projects. An

energetic particle could generate damage in CCDs and generate electron-hole pairs (3.6 eV/pair for silicon). Currently, a very large semiconductor integrated parametric test system is required to assess the overall functional sensitivity of CCDs to proton radiation. Radiation hardness verification testing of design changes, or effectiveness of radiation hardening in packaged devices is expensive and time consuming. These tests can also be performed with photons (light) having energy greater than that of the semiconductor bandgap (1.1 eV for silicon) because they produce electron-hole pairs in the device as inject parametric testers (for example, HP4145). In addition, a laser beam can locally (both vertically and horizontally) produce enough free carriers (6.1×10^{26} pairs/cm^3 for a 1-mW helium-neon [He-Ne] laser) to characterize integrated circuits without the attendant difficulties of other techniques; it is also quite economical. Accessibility to any single component in a circuit makes it suitable for routine testing of circuits for defect sensitivity, such as pixel cross-talks.

Virtual phase technology is a well-known technique for fabrication of large-area CCDs. Correct information of the gate oxide surface potential pinned to the substrate potential and of the maximum buried-channel potential are essential for a high charge-transfer efficiency in bulk channel CCDs [6,7]. The actual device-performance parameters, such as necessary gate potentials of the clock swing for optimum device operation, should be determined. By changing the gate bias for each fixed-source voltage, the built-in potential margin, as well as the clock well potential collapse, is directly observable.

In this report, the potential variation within the clocked well-virtual barrier (CWVB) and clocked barrier-virtual well (CBVW) of the dual-gate metal-oxide semiconductor/junction field-effect transistor (MOS-JFET) CCD test structures (TIJ J032) was measured as a function of gate bias voltage at a fixed source voltage under the local irradiation of the He-Ne laser. Since the drain voltage of a test structure at a fixed source voltages depends upon charges collected at the drain, the voltage variation of a drain at a fixed gate voltage depends upon the profile of the fabricated buried channel CCD and the physical defects of the structure when the laser power is constant. The potential in a buried channel silicon CCD test structure was also characterized after an irradiation of 250 krad of 250 keV protons(10^{12} protons/cm^2) at room temperature to observe the nature of the defects due to proton radiation. For quality assurance of the device reliability against potential operational failures, preliminary test results were also discussed, comparing them with the total device performance collected by a parameter tester so as to understand the physical and functional optimization of the devices.

2. Test Structures

Figure 1 shows an overall optical view of the device, while Figure 2 shows the dual-gate MOS-JFET test transistors. Five aluminum wires were bonded to the pads of bulk (B), source (S), gate (G), drain 1 (D1) and drain 2 (D2), and to respective posts for these measurements. Closeup scanning electron microscope (SEM) views of the test structures (CWVB and CBVW) are also shown in Figure 3. These transistors correspond to the virtual well-clocked barrier and clocked well-virtual barrier regions in the virtual-phase CCD, and are fabricated at the same time as the virtual-phase CCD imager. These transistors are used to measure the potential energy of barriers and wells, as affected by the variations of the gate bias. Using these devices, the clocked well potential collapse, as well as the built-in potential margin necessary to develop lateral fringing fields, is directly observed. In addition, values for potential

well levels and the necessary clock swing for proper device operation are easily determined. These devices, therefore, serve as efficient process-monitoring tools.

A cross-section of a two-phase CCD, along the charge-transfer channel, is shown in Figure 4. In this design, charge-transfer directionality is achieved by placing suitable implants under various portions of the phase electrodes, as indicated by "+" or "–" signs. These implants produce permanent potential barriers and wells which are raised and lowered by application of the appropriate voltages on the overlying gates to provide complete and unidirectional charge transfer. In a virtual phase device, the electrode which is maintained at dc potential is not built above the gate dielectric as a separate structure, but rather is built directly into the silicon surface and is biased at the substrate potential.

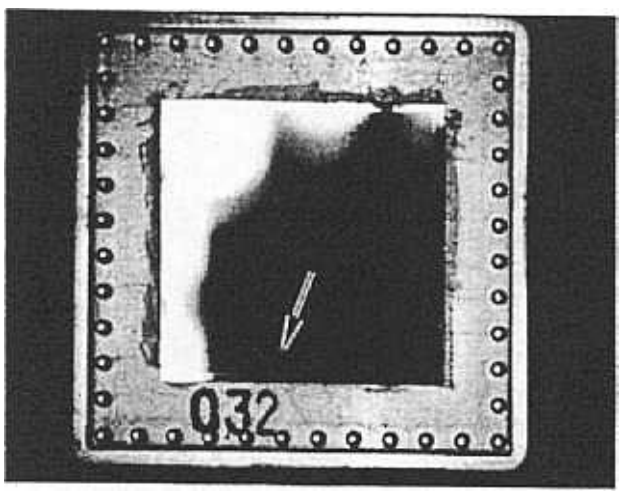


Figure 1. Overall optical view of the device, TIJ J032. The arrow indicates the test structures.

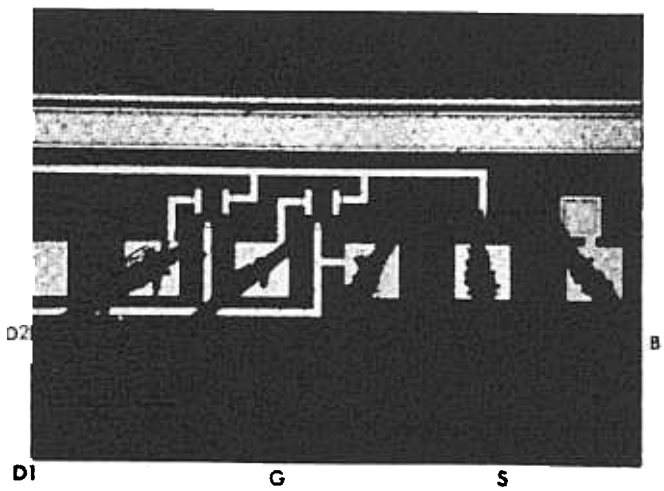


Figure 2. Close-up view of the test structures. Five wire bondings were made for these tests: B is bulk, S is source, G is gate, D1 is the drain of the CWVB, and D2 is the drain of the CBVW.

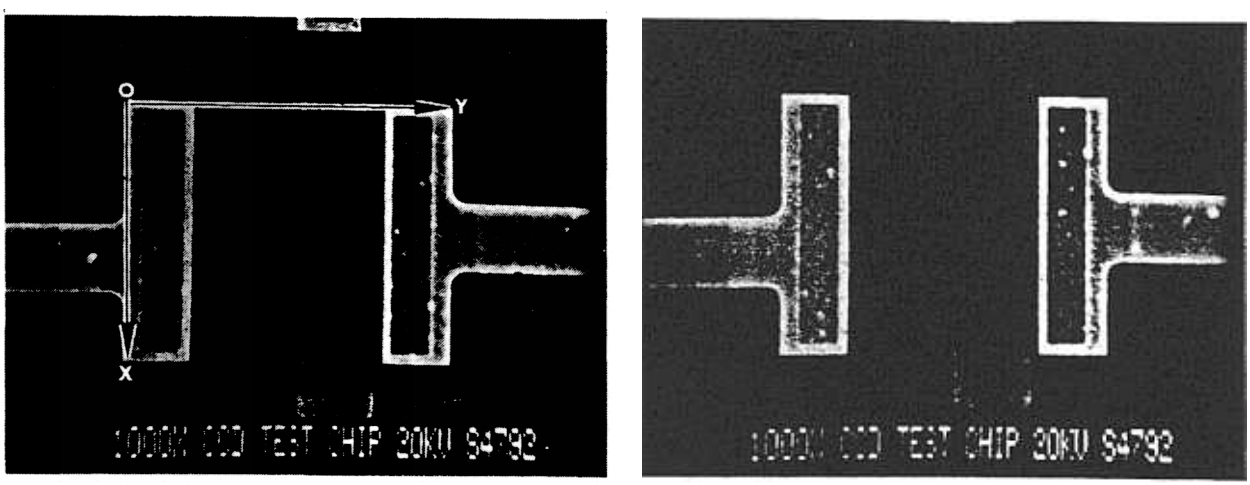


Figure 3. SEM views of the test structures CWVB, CBVW. The arrows indicate the areas scanned by the advanced laser scanner for the drain potential variation.

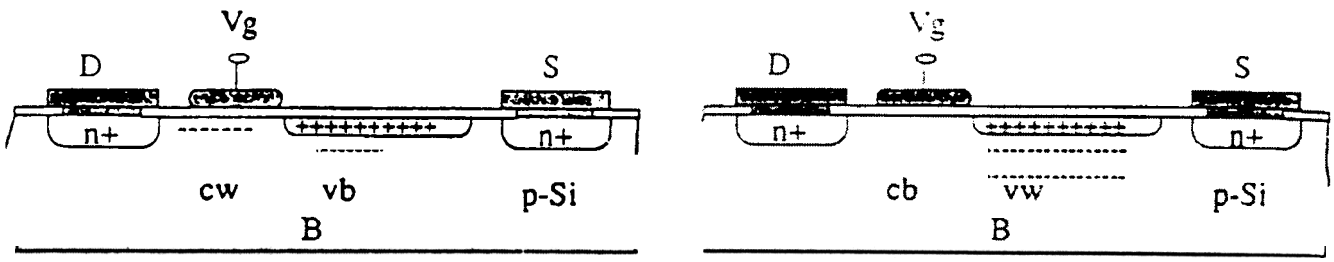


Figure 4. Schematic cross-section diagram of the test structures.

One important feature of the buried channel structure to note is that electrons are stored away from the surface, and, therefore, they are free from the undesirable influence of surface scattering and traps. Another important feature of the buried channel structure is called the potential pinning phenomena. As the gate potential (*VG*) is lowered toward a more negative bias, the surface potential (*VS*) also is lowered until it reaches the point where *VS* = 0. When this occurs, the holes from the channel stops will flow across the surface and prevent further lowering of *VS*. Therefore, *VS* is pinned to zero. Since the holes can occupy only a very thin region of space near the surface of the silicon, the potential profile within the silicon will not be affected by the number of holes needed to compensate for any additional field induced by the gate. As a result, the maximum value of *VG* also will be pinned to some value, regardless of any further lowering of the gate potential. Since the pinned potential profile of the buried channel structure stays positive, the signal charge can be effectively transferred under the accumulated layer of holes. The holes accumulated in the thin surface layer act as a virtual gate for the underlying buried channel region.

3. Laser Scanner Test

The multipurpose microelectronic advanced laser scanner (MMEALS), as shown in Figure 5, is based on the principle that photons that have energies greater than the gap of the semiconductor can be absorbed, producing electron/hole pairs in the device under test. In the MMEALS, light from a continuous He-Ne laser beam is focused at selected locations on an integrated circuit to test for vulnerability of those locations to device performance. The beam can be scanned from one location to another in a controlled manner to identify sensitive areas. The wavelength and energy of the laser beam can be tuned to vary the effective depth of penetration of the photons so as to probe the layers of the circuit with great sensitivity. It is an opto/electro/mechanical apparatus for nondestructive testing of integrated sensors, logic circuits, and other microelectronic devices. The MMEALS is, in addition, a multipurpose diagnostic system that can be used to determine ultrafast time response, leakage, and electrical overstress in complex integrated circuits (ICs) utilizing other device information, such as mask patterns and device parameters. Most notably, it can be used to simulate the effects of heavy ions accelerated to high energies and then determine the susceptibility of a digital device to single-event upsets (changes in stored bits unaccompanied by significant permanent damage) as well as latchups [3].

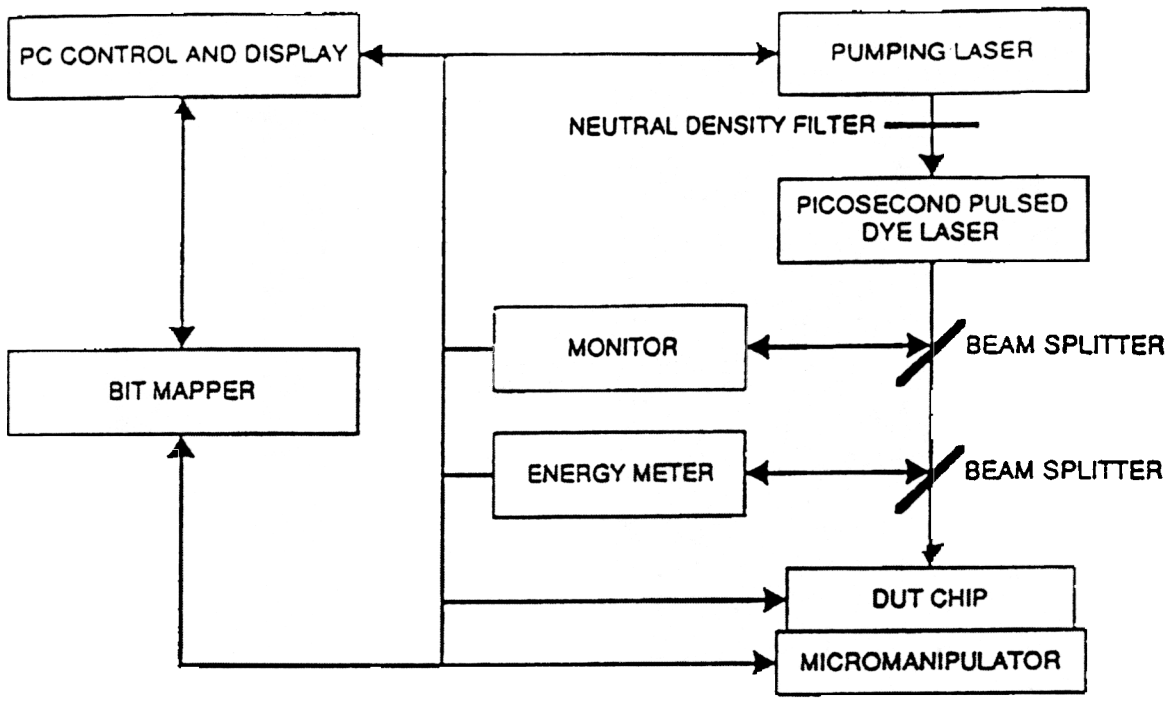


Figure 5. Test setup of the MMEALS.

By slowly scanning the laser beam on the microelectronic components in an integrated circuit, the most sensitive component of the integrated circuits can be identified and plotted on an optical bit map of the device. Such variables as the laser energy deposited in the device under test, and the threshold value causing faulty performance can be plotted and used to explore methods to optimize device performance [8].

Because of fundamental differences between irradiation by laser at an isolated portion of an electric component and injecting carriers into the device by electrically biasing the device, caution must be exercised in interpreting the results of tests on the MMEALS. For example, one difference is that the track of electron/hole pairs injected by a semiconductor parameter analyzer reflects the performance of the whole device, while that of the carriers generated by a laser beam irradiated on a component represents only the performance of a local part of the integrated device. Another difference is that the density of charge carriers produced by the laser beam decreases approximately exponentially with depth of penetration, while that of an injected carrier does not. Still other differences involve energies and mechanism of interaction with the semiconductor structure and distribution of charge carriers. Despite these differences, initial results show excellent agreement between parts characterized by both the laser and parametric analyzer. Thus, the new MMEALS represents both an efficient way of characterizing parts and, for the first time, identifying key elements of concern in the local structure of a given device.

4. Potential Distribution of the Test Structures

The drain voltage of the test structures (CBVW and CWVB) of the dual-gate MOS-JFET CCD (TIJ J032) was measured both by a parametric tester and the MMEALS. The details of the parametric test condition of HP4145 are shown in Tables 1 and 2. The gate voltages were changed over the range from –8.0 V to + 40 V. The voltages of the drain at

several fixed-gate voltages under a source voltage of 10 V were monitored by scanning a focused He-Ne laser beam (wavelength: 632.8 nm) over the test transistors. The beam diameter of the laser is about 2 μm, and the power of the laser is one μW.

Figure 6 shows the drain-voltage variation of the CBVW at 10 V of source voltage with respect to various gate voltages as measured by the MMEALS. For this measurement, the clocked barrier was pinned at *VG* = –5.5 V to *VD* = 2.0 V, while the *VD* saturated to 4.4 V at *VG* = –3.0 V. This indicates that the gate voltage should be regulated by the system clock for the needed potential barrier shift from lower than –5.5 V to higher than –3.0 V for the effective charge transfer for this device.

Table 1. Test conditions of the drain voltages of CBVW versus gate voltages.

Table 2. Test conditions of the drain voltages of CWVB versus gate voltages.

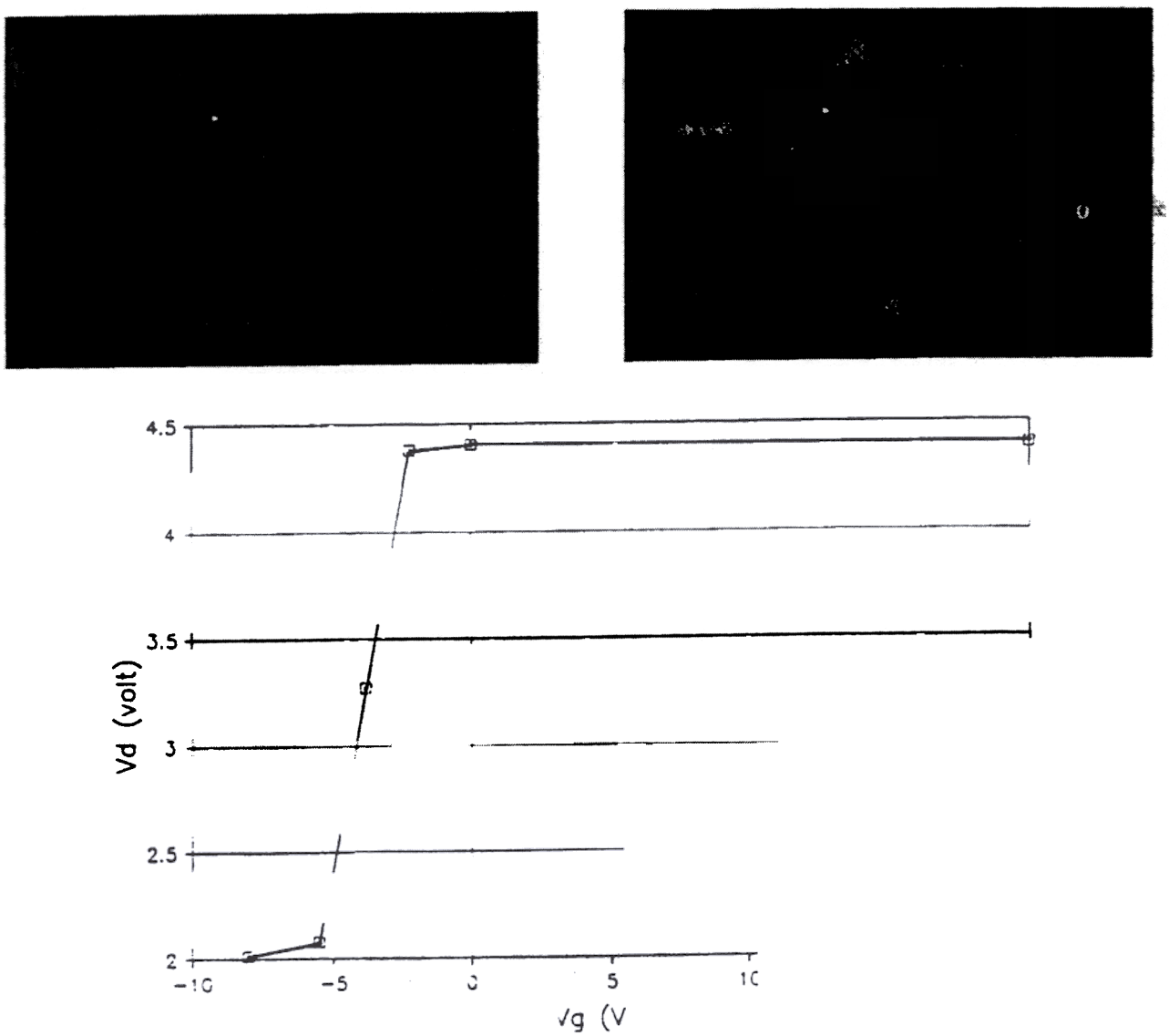


Figure 6 Discrete measurements of the change of drain voltage (*VD*) of the CBVW with respect to gate voltage (*VG*) under He-Ne laser irradiation.

Similar results for the test structure of the CWVB are shown in Figure 7. *VD* was pinned to be 2.1 V at *VG* = –6.0 volts, and *VD* was saturated at 2.7 V, when *VG* = –4.0 V for the MMEALS tests.

The potential distribution of the test structures at a fixed source voltage of 10 V was measured by monitoring drain voltages at various gate voltages ranging from –8.0 to 2.0 V. The background data, which were taken using no laser irradiation, are shown in Figure 8(a). The topological variations of the drain voltages at *VS* = 10 V under different gate bias voltages are displayed in Figures 8 and 9. The drain voltages are shown on the z-axis with respect to the location of test structures when the laser scans over the test structures.

Note that the scales of z-variables of all plots are the same (700 mV) for a direct visual comparison, but the ranges of the z-axes are shifted according to the average drain voltages. The measured drain voltages were shown on the z-axis with respect to the area ($X \times Y = 50\ \mu m \times 60\ \mu m$) scanned by the laser. Any sudden deviation from the average drain potential can be interpreted as physical defects of a device. No deviations were found in this test. Had there been such deviation, however, the nature of the defects could have been analyzed, using these test results as a guideline by further destructive analysis. This information could then be utilized for screening high-reliability imaging systems for space application.

Note also that the clocked barrier that collapsed at *VG* became higher than –3.8 V for the CBVW, as shown in Figure 8(d), while the clocked well was collapsed when the gate voltage became higher than –4.8 V for the CWVB, as can be seen in Figure 9(c). This means that the MMEALS can be used not only for optimizing the device parameters, but also as an effective manufacturing tool in CCD fabrication.

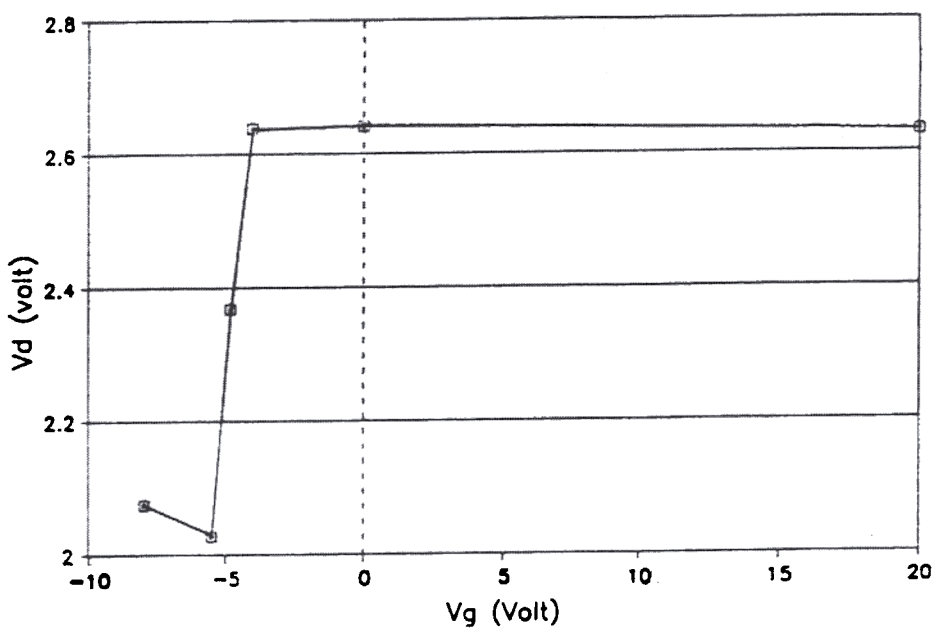
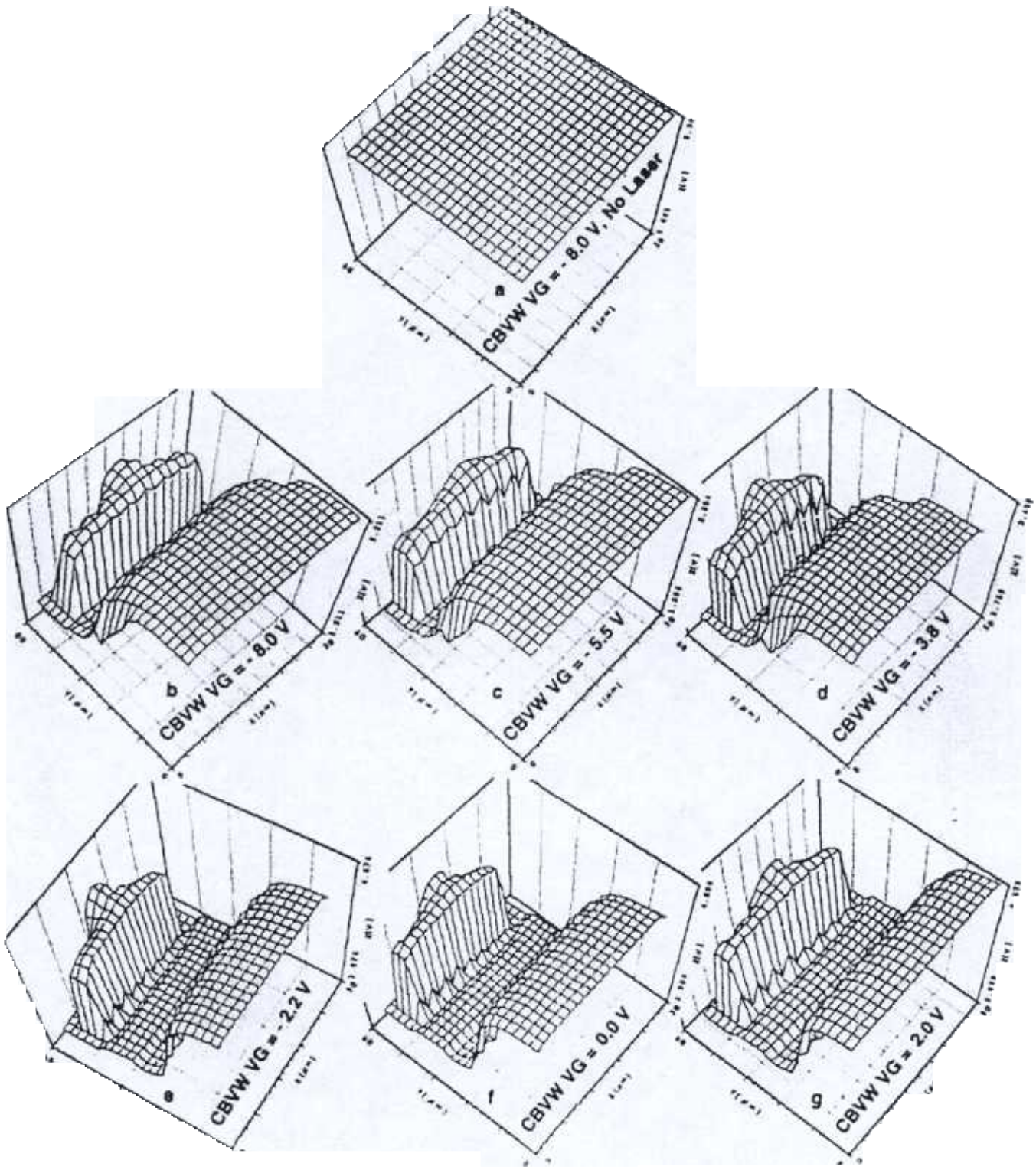
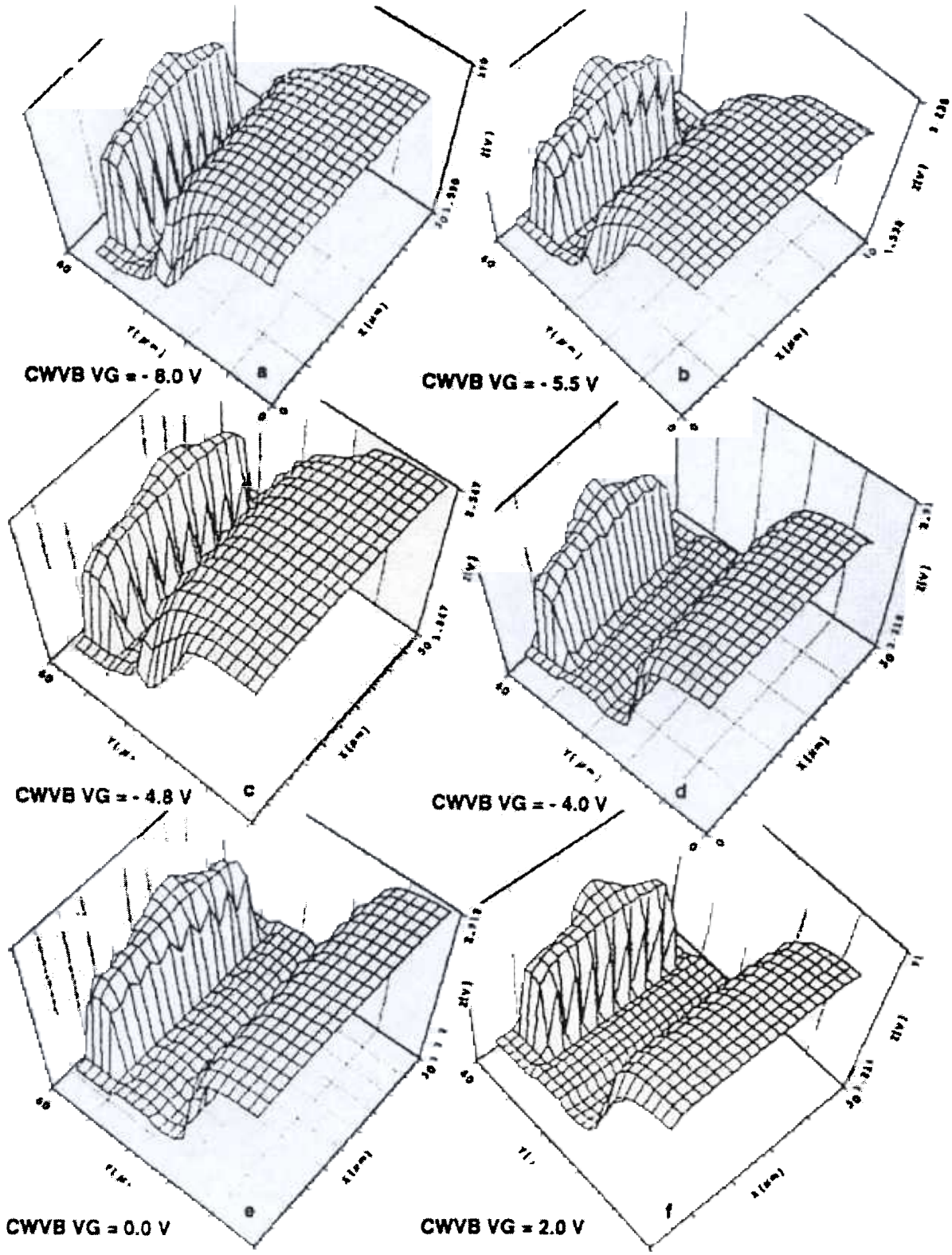


Figure 7. Discrete measurements of the change of drain voltage (*VD*) of the CWVB with respect to gate voltage (*VG*) under He-Ne laser irradiation.



Figures 8(a)–(g). Topological display of the drain voltage at several different gate bias voltages for the test structure CBVW.



Figures 9(a)–(f). Topological display of the drain voltage at several different gate bias voltages for the test structure CWVB.

5. Effects of Proton Damage

Two general types of CCD radiation damage critical to the CCD have been previously reported as ionization and bulk damage. Recent analytical and experimental work has provided new insights into the production of damage sites in silicon CCDs by energetic particles [2]. In order to examine the change of the potential structure, the test structures were irradiated by protons at room temperature (10^{12} protons at a flux of 1×10^8 protons/s cm^2). In this experiment, the protons are approximately monoenergetic at 250 keV. The damaged test structure was then characterized using both the MMEALS and the parametric tester. The clocked well was collapsed (as usual) when the gate voltage was lowered by about 1.0 V, which is the same as before radiation, as shown in Figures 8(d) and 9(c). Bulk damage could be induced in the silicon material on which the device is fabricated. Bulk damage occurs when radiation events displace silicon atoms in the lattice structure, creating bulk traps. In addition, electrons from the silicon valence band can thermally hop to trapping centers, generating a high, dark current and creating hot pixels or dark spikes. However, no significant shifts of the gate voltages between the pinning and saturation voltages were observed 17 days after the radiation, as shown in Table 3. This is probably because the radiation was performed at room temperature.

Table 3. Change of the gate-voltage shifts from pinning to saturation of the test structure CWVB after proton radiation.

Annealing time (hr)	0	12	139	374	422
Shifts (V)	1.11	1.20	1.07	1.06	1.00

Figure 10 shows the variation of *VD* of the CWVB with respect to *VG* after proton irradiation. The depth of the clocked well at the same gate voltage of –4.0 V was reduced to 29 percent (0.2 V) from the initial potential depth of 0.7 V. When electron-hole pairs are generated by energetic particles passing through the insulator of the gate oxide, ionizing damage occurs. The charge created can be trapped in the insulator, resulting in a flat-band shift in the clock-operating voltages to the CCD, which cause a degradation of the charge transfer efficiency (CTE). Charges built up in the oxide become trapped at the gate Si-SiO2 (silicon dioxide) interface [4]. These results may reflect the degradation of the potential profile of the test structure after proton irradiation, regardless of their origins.

Table 4 shows the shifts of threshold voltage of the test structure after proton irradiation at room temperature. Initial increase of threshold voltage followed by decrease below the initial voltage has been observed, as reported elsewhere. Further analysis is forthcoming for the performance related to this observation.

C. SIGNIFICANCE OF THE RESULTS

Drain voltages of the test structure of dual-gate MOS-JFET CCD (TIJ J032) were measured by an advanced laser scanner. The voltage variation of the test structure at various source and gate voltages was plotted with respect to the scanning laser position. In this report, a fine, continuous, constant-energy He-Ne laser beam of the MMEALS is utilized for the characterization of local variation of sensor performance within the test structure. The results

were compared with the performance of the whole device by a semiconductor parameter analyzer. The threshold gate voltage of the device for a fixed-source voltage was determined by measuring the drain voltage with respect to gate voltages while the laser illuminated the device. Such threshold variables were then used to collect local responsiveness of the test structure to find defects most vulnerable in design and fabrication while the micron-size laser beam was scanning the whole test structure in a controlled manner. Preliminary results show an excellent correlation between specifications of the same parts characterized by the semiconductor parameter tester and those by laser. Furthermore, variation of the drain voltage closely reflects the details of the fabricated test structures. Thus, the new MMEALS technology could be used in testing design efficiency and performances of the device, which are vital for the manufacture of highly goal-oriented microelectronic CCDs or active pixel sensors.

RESPONSIVITY MAP OF A TEST STRUCTURE(CWVB)
Dual Gate MOSJFET CC , TIJ S/N JA32
119 Days After 250KeV 1E12 Protons/sq. cm at RT

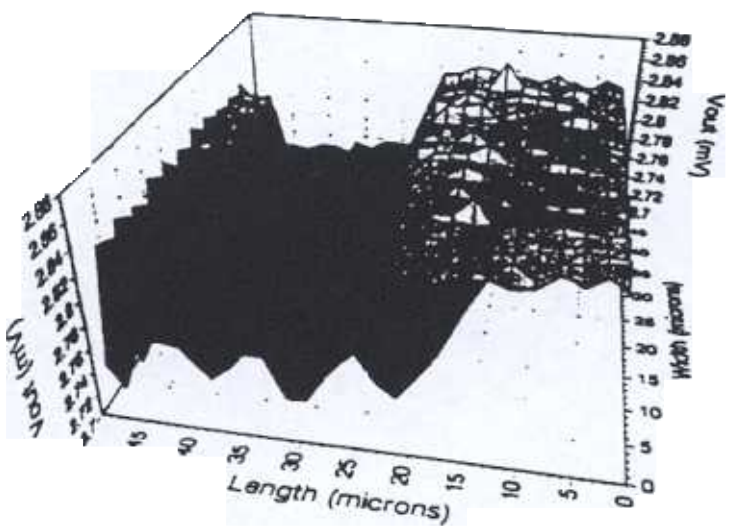


Figure 10. **Topological map of the potential distribution of the CWVB after 10^{12} proton irradiation at room temperature. The device functioned properly even after the irradiation. However, the built-in potential of the test structure was degraded to 29 percent, as shown in Table 4.**

Table 4. **Change in the built-in potential depth of the test structure CWVB after proton irradiation.**

Annealing time (h)	0	1.6	21	120	422
Depth (V)	0.72	0.16	0.14	0.14	0.14

D. ACKNOWLEDGEMENTS

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E. PUBLICATIONS

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